Investigation of Thermal Crosstalk Between SOI FETs by the Subthreshold Sensing Technique

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***Abstract*—Experimental–modeling investigation of the transient thermal crosstalk between the field-effect transistors implemented on a silicon-on-insulator substrate is reported. The measurements were performed using a high-speed electrical pulse–probe sampling technique, which allowed detection of thermally modulated subthreshold currents. The technique achieved a temperature resolution of ~50 mK, a time resolution of 5 ns, and a temperature sensitivity of ~0.6 μA/K. The finite-element method was used to solve the heat diffusion equation and to obtain the temperature profiles for the given device structures. The combined high-resolution experimental–simulation approach allowed the study of the thermal crosstalk between two adjacent devices and probe the local temperature at different locations of the structure. The effects of the interface quality, layer thickness, material selection, and interdevice spacing on the heat diffusion and device performance were investigated in detail.**

***Index Terms*—Heating, MOSFET, pulse-probe, silicon-on-insulator (SOI), transient.**

I. Introduction

HEAT generation is a major design concern for the optimization of the downscaled silicon-on-insulator (SOI)-based devices [1], [2]. Self-heating effects have become an important reliability issue in the bulk and SOI-based CMOS circuits affecting electrostatic discharge [3], [4] and causing excess heat generation in the MOSFETs. In the high-level integrated circuits, the problem of thermal crosstalk is also gaining importance [2], [5]. This means that not only the heat-generating device but also its neighboring devices suffer performance degradation. It is important to be able to characterize the full thermal transient behavior since the chip thermal activity fluctuations tend to be on the same timescales as typical thermal time constants, resulting in peak transient temperatures that may well exceed steady-state average temperatures. There have been few attempts at transient thermal characterization of CMOS devices with recent notable advances [6], but this paper is the first comprehensive study resolving detailed thermal transients for CMOS devices.

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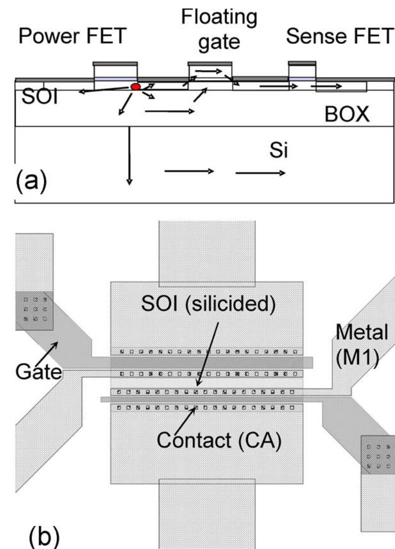

Fig. 1. (a) Schematic of the device test structure and various possible heat conduction paths. (b) Layout showing the two 10-mm-wide transistors in the test site with gate lengths of 0.6 μm (top) and 0.25 μm (bottom) separated by the silicide gap.

This paper describes the results of the investigation of the thermal crosstalk between two FETs implemented on an SOI substrate. The developed technique measures the temperature rise in the device, which generated the heat wave ("power" FET), and monitors it away from the heat source (with the "sense" FET) at several different locations. The effects of the specific features of the device structure, such as floating gate (FG), shallow trench isolation (STI), SOI substrate, and variable dimensions of these structures on heat propagation between the devices, were systematically investigated. The test structures used in this paper include partially depleted SOI n-FETs, which consist of two n-FETs connected back-to-back, as shown in Fig. 1(a). The FETs both have a width of 10 μm and gate lengths of 0.6 and 0.25 μm, respectively. There are a total of 15 such pairs with varying design parameters [see Fig. 1(b)]. The examined set of the test structures had different material enclosures of variable lengths between the two FETs. The tested device structures could be divided into four main types. The structures that are referred to as I (for insulator) have STI between the two FETs, whereas those referred to as PC have a poly-Si FG between the two FETs.

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TABLE I
DEVICE LAYER THICKNESSES AND THERMAL CONDUCTIVITIES

	Thickness (nm)	K (W/mK)
Oxide overlayer	300	1.38
Poly-Si Gate	100	125
Gate oxide	1.5	1.04
SOI	40	40
Silicide	40	40
Buried Oxide	140	1.38
Si	16000	155

OP structures have an n^+ doped SOI layer, whereas the RX structures have silicide between the two FETs.[1] Various device layer thicknesses are summarized in Table I.

The measurement and data analysis procedure involved several steps. First, a fast pulse circuit was used to provide a rapid switching of the transistors while maintaining the proper time synchronization between the heating power pulse and the sensing pulse. Second, the subthreshold current is measured. Third, the transmission line elements are used to attenuate the reflections arising from high-frequency signals. The data extraction includes a temperature calibration procedure in order to obtain the temperature sensitivity of the subthreshold currents. Finally, finite-element method (FEM) modeling was used to calculate temperature profiles in the device structure, study transient heat propagation, and compare the modeling results with the experimental data.

II. EXPERIMENTAL TECHNIQUE

The typical thermal time constants in Si for self-heating are on the order of hundreds of nanoseconds [7]. Thus, in order to study the transient heating effects, fast pulses need to be employed. A dual-channel pulse generator (Agilent 81134A) was used for this purpose. The channels were synchronized by entering the appropriate channel delay to allow the "power" transistor enough time for heat generation before the sensor transistor is switched on by the pulse generator. The pulsewidths of the "power" and "sense" transistors were digitally programmed. The circuit of the experimental setup is illustrated in Fig. 2.

The power pulse generator was set to a timing of 2 ns/bit. All the cables and connections carrying signals were of a 50-Ω subminiature-A-type coaxial with a bandwidth greater than 10 GHz, matched to a 50-Ω load. The attenuators were used to reduce the effects of multiple reflections between the unterminated probe heads and other discontinuities in the circuit. The 35-GHz signal–ground–signal microwave probes were used for the application and collection of the pulse signals to the "power" and "sense" FETs. An HP 54542C oscilloscope with a bandwidth of 500 MHz was connected to two FETs to monitor the power and sense pulses, particularly in regard to

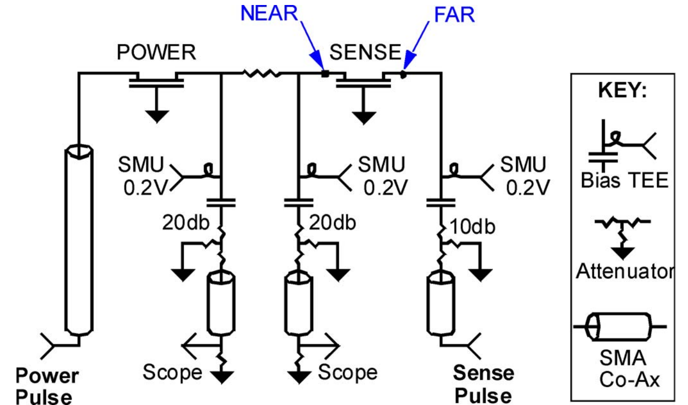

Fig. 2. Circuit diagram of the experimental setup for the case where the "power" and "sense" FETs can be electrically connected and where sensing is done at the FAR terminal of the "sense" transistor.

pulse timing but not used for temperature measurement. It also provided the 50-Ω load and, hence, did not show any spurious signal due to the reflections. The bias tee was used to hold the drain bias constant while passing the ac output signal to the oscilloscope. The data were collected using the source–monitor units (SMUs) of an HP 4145B parameter analyzer. Low-pass filters, each consisting of a ∼300-Ω series resistor and a 0.2-μF shunt capacitor, reduced the disturbances due to residual high-frequency pulses on the SMUs. The pulse generator, power supply, SMUs, and oscilloscope were programmed to be computer controlled. This allowed for fully automated measurements over a prolonged period of time with a high level of precision. Electroless copper deposition provided a good contact between the probe and the device metal contact pads during the measurement scans.

III. EXTRACTION OF THE THERMAL SIGNAL

A. *Subthreshold Sensing Technique*

The principle of the detection of the temperature rise using FETs in the subthreshold mode uses the fact that the subthreshold (sub-V_t) current exponentially depends on the temperature and can be written as [8]

$$I_D = \mu_{\text{eff}} C_{\text{ox}} \frac{W}{L}(m-1)\left(\frac{kT}{q}\right)^2 e^{q(V_g - V_t)/mkT}\left(1 - e^{-qV_{DS}/kT}\right). \quad (1)$$

Here, μ_{eff} is the effective mobility at some average gate and drain fields, C_{ox} is the oxide capacitance per unit area, L is the channel length, W is the width of the device, m is the body-effect coefficient, T is the temperature, k is the Boltzmann's constant, q is the electron charge, V_t is the threshold voltage, and V_g is the gate voltage of the FET.

One can see from (1) that any temperature T fluctuation in the neighborhood of the transistor operating in the sub-V_t regime gives rise to the thermally modulated subthreshold current with the exponential term dominating the temperature sensitivity when the device is operating well below the

[1] Acronyms are historical and refer to the physical design shapes used to define that feature: RX for the oxide isolation (or, inversely, the SOI island), PC for the polysilicon gate, and OP for the silicide protect mask.

threshold. Negative power and sense pulses are applied to the source terminals of the "power" and "sense" transistors, respectively, with a varying delay between them. The sense pulse acts as a sampling window, and the output is a convolution of the sense pulse and the thermal response due to the power pulse. Note that both power and sense pulses have to be short in order to catch the rising edge of the thermal transient. Typically, the sense pulses were half the duration of the power pulses.

In order to measure the signatures of T change in the subthreshold current with the previously described experimental setup, one needs to the implement the following steps. First, one has to perform the calibration of the subthreshold current I_D to extract its sensitivity to temperature. Second, one has to select the right operating voltage range—both for the "power" FET (in order to generate enough heat) and the "sense" FET (in the subthreshold region)—so that the signature of the thermal transient can be detected. An alternative regime for the detection of the heat wave, which is different from the subthreshold current, will be discussed in the next section. The estimated value of the subthreshold current, which carries the signature of the heat wave, is on the order of few tens of nanoamperes, resulting in the need for the sophisticated noise reduction techniques to extract the thermal signal. The noise reduction techniques used in the experiments will be described further on.

B. Temperature Sensitivity Measurements

To extract the I_D–T sensitivity, the current–voltage (I–V) characteristics of both FETs were measured using the temperature-controlled chuck. The pulsed I–V characteristics were recorded for the 0.25- and 0.6-μm FETs at the chuck temperatures of 12 °C, 18 °C, 24 °C, and 30 °C. These data were used to extract the rate of change of I_D with respect to the temperature rise. Fig. 3 shows the I_D–T sensitivity plot for the 0.25-μm FET. It is clear from the plot that there are two modes of thermal sensitivity, namely, the subthreshold (low-V_g) mode associated with a positive temperature sensitivity and the above-threshold (high-V_g) mode of heat sensing associated with a negative temperature sensitivity.

The underlying physics of the two modes is different. In the low-V_g mode, the sensing of heat by I_D is based on the thermally activated carrier injection, as given by the exponential term in (1), whereas the current–temperature sensitivity in the high-V_g mode is governed by the carrier mobility degradation [9]–[11], due to the increased electron–phonon scattering at higher temperatures. The subthreshold sensing of heat requires a very careful experimental setup, a refined measurement technique, and noise reduction. However, it is also a more reliable and accurate approach because the coupling due to the electrical effects, such as high-field effects, is minimal since the device is exponentially turned off when its output current is not being sampled. It is particularly suited for spatial probing since the current is mainly determined at the point of injection, rather than by the properties integrated along the entire device. In this paper, the temperature was measured at the junctions near (NEAR) and far (FAR) from the heat source using this subthreshold sensing technique. The comparison of the current–temperature sensitivity curves for two FETs

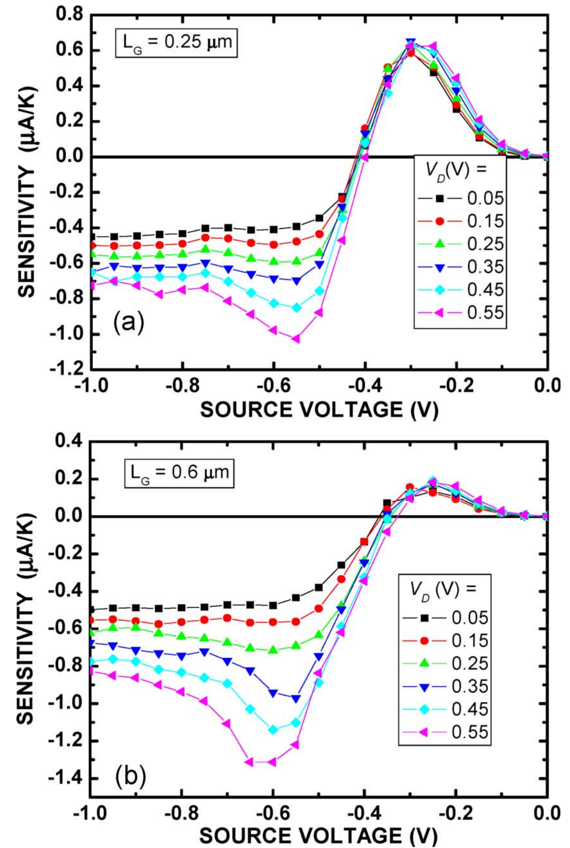

Fig. 3. Current–temperature sensitivity curve shown for the (a) 0.25-μm gate length FET and (b) 0.6-μm gate length FET.

(0.25 and 0.6 μm) revealed that the 0.25-μm FET has a higher current–temperature sensitivity. This could be due to the nonlinear doping along the length of the FETs caused by the halo-type implant or increased preponderance of the ballistic transport at shorter gate lengths in the subthreshold regime. For this reason, the 0.6-μm FET was predominantly used as the "power" FET to generate the heat wave, and the 0.25-μm FET was used as the "sense" FET to measure the temperature. The operating subthreshold voltage was carefully selected from I_D–T to be at the peak of the temperature sensitivity curve. Since the grounded-gate probe configuration was used, the source voltage corresponding to the maximum I_D–T sensitivity gives the V_g value. Referring to Fig. 3, the drain and source voltages are both biased at a small positive value, during the quiescent period, in order to provide a negative V_{GS} at zero V_{DS}. During a negative pulse applied to the source, both V_{GS} and V_{DS} are biased positive, by the same amount, relative to their quiescent values. The pulse was adjusted so that the value of I_D measured by the SMU and after taking into account the duty factor is equal to the current value for the maximum temperature sensitivity ($\sim$100 μA). A peak voltage swing of -2.5 V (including the voltage doubling at the unterminated probes) was applied to the source of the power FET. This value well exceeds the maximum operating voltage for this technology but is permitted because the duty factor is low. When pulsing the NEAR terminal of the "sense" transistor, the same pulse is applied to the drain of the power transistor to equalize the voltages and prevent the current flowing between them.

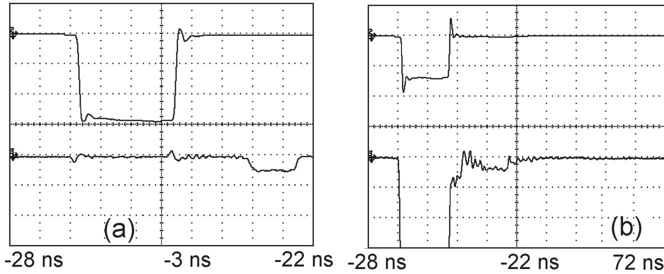

Fig. 4. Transient current in the power transistor (top) and sense transistor (bottom), showing cases for (a) insulating and (b) conducting connections between the two transistors. Horizontal scales are 5 and 10 ns/div, respectively.

C. Sampling Technique for Noise Reduction

In the subthreshold mode, the output signal is very small, and the environment is noisy. The sense current is $\sim$100 μA into 50 Ω (i.e., sense voltage $\sim$5 mV). However, the duty factor of 0.39% (8-ns pulsewidth) is small. This was designed to avoid the carryover heating due to the power pulse applied in the previous pulse cycle. Variation in I_D due to temperature is $\sim$600 nA/K (see Fig. 3), which corresponds to only 60 nA ($\sim$1000 times less than the input sense pulse) for a 0.1-K temperature rise. For this reason, even small reflections and oscillations of RF signals can result in the loss of the embedded heat signal. Thus, it is important to implement the background noise subtraction and reduction in order to trace the signature of the thermal transient.

In addition to the previously described circuit techniques, a digital lock-in technique was used to discriminate against noise and drift. This technique is based on the sampling of the high-frequency pulses that are applied to the "power" and "sense" FETs. The power pulse was switched on and off at a 1-Hz rate. The "sense" FET output signal was measured at each instance (i.e., during both ON and OFF cycles), and the difference was taken. A higher switching rate could not be implemented due to the programming limitations of the pulse generator. The procedure was iterated several times and averaged to extract the embedded thermal signal value at each delay. This insured the reduction of noise and increased the temperature resolution, which is defined as

$$R_T = \frac{S_N}{\sqrt{D_F t}} \tag{2}$$

where S_N is the noise spectral density, D_F is the duty factor of the sense pulse, and t is the total measurement time. For example, in the case of the FG structures, R_T is 0.065 K (or $\sim$50 mK). The measurements involve the scan over many delay points in order to record the complete thermal transient. The scan over a large range of delay points could give rise to the long-term drift component of noise due to the time-dependent change in the environmental factors. Averaging of multiple sweeps was tried to reduce errors, but in practice, this turned out to be unnecessary.

In Fig. 4(a), one can see the output "power" and "sense" transistor current signals for the I-200 test structure. It shows the 16-ns input power pulse (top) and the 8-ns sense current pulse (bottom). Only the small disturbances are seen due to the capacitive coupling between the two FETs. In the case of OP test structures [Fig. 4(b)], the disturbance is much larger due to the resistive connection via the doped SOI. Nevertheless, even in the latter case, the transient quickly recovers, and the sense pulse is clearly visible. In order to measure the thermal transient, sense pulses have to be resolved to an accuracy of $\sim$0.1%.

IV. Simulation of Transient Heat Transport

The simulation of the thermal transients through the device structures was carried out by solving the 2-D heat diffusion equation (since the width of the device $W = 10\ \mu\text{m} \gg L = 0.25 - 0.6\ \mu\text{m}$) using the FEM implemented in the FEMLAB software package. The temperature rise in the device structures was determined by solving the nonlinear heat flow equation, which is written as [12]

$$c(\vec{r},\theta) \times \rho(\vec{r},\theta) \times \left(\frac{\partial\theta(\vec{r},t)}{\partial t}\right) = \text{div}\left(\kappa(\vec{r},\theta)\right) \times \text{grad}(\theta) + Q(\vec{r},\theta) \tag{3}$$

where c is the specific heat, $\theta(= T - T_o)$ is the temperature rise, $\vec{r}$ is the position vector, Q is the heat flux, κ is the thermal conductivity, and t is the time. An adaptive mesh was used to determine the mesh size from the structure geometry and was refined with high accuracy. The bottom of the substrate (approximated by a plane 16 μm from the top surface) is maintained at 300 K. The side boundaries were thermally conductive with the heat flux $(n \times \kappa\nabla T = \overrightarrow{Q})$. The internal boundaries were assumed to be continuous $(\kappa_1 \nabla T_1 = \kappa_2 \nabla T_2)$. The layer thickness and thermal conductivity values used are listed in Table I. Note that the thermal conductivity for the SOI, i.e., $\kappa_{\text{SOI}} = 40$ W/mK, is much smaller than the bulk value of the thermal conductivity for Si, i.e., $\kappa_{\text{Si}} = 155$ W/mK. The simulations took into account the reduction of the thermal conductivity in the SOI and in the gate oxide layers.

V. Results and Discussion

In order to understand the effect of the device structure and materials on heat removal, the measurements were made on four different kinds of devices with four different materials between the "power" and "sense" FETs. Each kind of device had samples with various lengths of the intermediate structure (FG, STI, silicide, or SOI). The heat flux generated by the "power" FET propagates through the structure with diffusion-limited transport, which differs from one material to another. The results of the simulations clearly show that the heat diffusion through different layers strongly depends on the κ values in the respective layers. Heat diffuses faster and over larger distances in the gate region and diffuses over shorter distances in the SOI or silicided regions (note that $\kappa_{\text{silicide}} \sim \kappa_{\text{SOI}}$). The weakest diffusion was observed in STI. These results are in line with the decreasing k values, i.e., $\kappa_{\text{poly-Si}} > \kappa_{\text{SOI}}(\sim \kappa_{\text{silicide}}) > \kappa_{\text{SiO}_2}$. Simulation in Fig. 5 shows that the propagation of heat wavefront is remarkably different in the silicided, FG, and STI device structures with three distinct

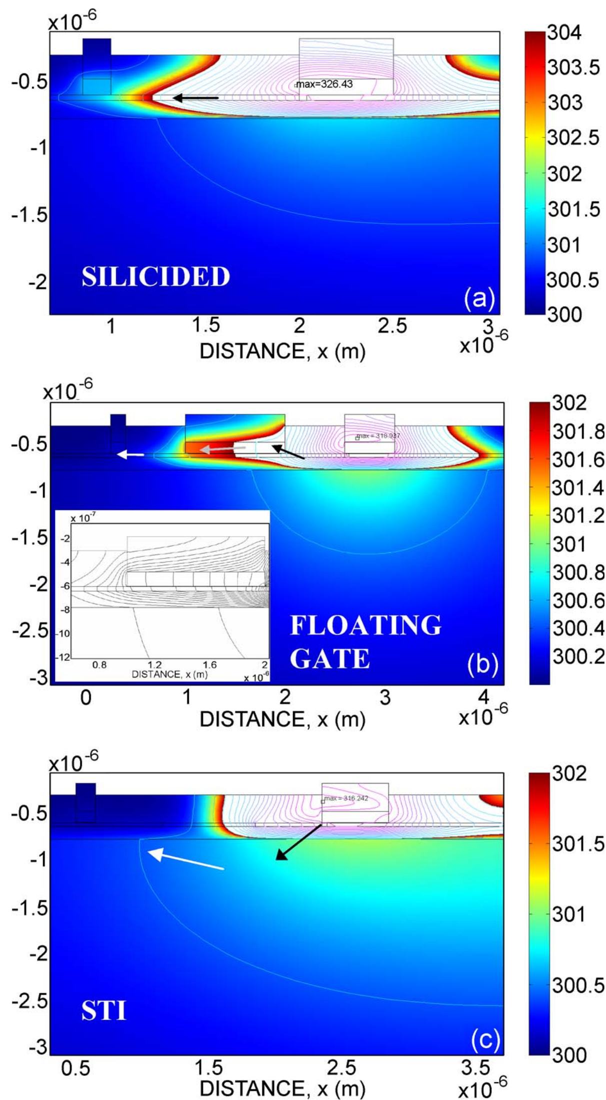

Fig. 5. Simulated temperature profile in dual CMOS SOI FETs connected by the (a) zero-length RX structure at 10 ns and (b) 1.1-μm-long FG structure at 20 ns. Inset in (b) shows the effect of thermal resistance due to FG, as illustrated by retarded temperature contours in the FG region. (c) STI of 0.7 μm at 30 ns. Arrows point to the dominant heat conduction path.

dominant conduction paths. While the heat wavefront propagates through the SOI layer in the silicided structure, it rushes through the poly-Si FG in the FG structure, whereas in the STI structures, it bypasses the insulator gap via the Si substrate. Fig. 5(a) shows the heat propagation in the silicided structure with minimum device separation length (zero additional length) at $t = 10$ ns postpower pulse. The heat source location is the drain of the 0.6-μm "power" FET. The simulation results show that in this case, maximum heat spreading laterally takes place in the plane of the SOI. This would contribute to the greater thermal crosstalk. Fig. 5(b) presents simulation results showing the heat front rapidly progressing along an FG. As one can see, the heat wave first diffuses into the gate region, which then acts as a secondary heat source. Interestingly, the FG has another competing effect. It also adds a thermal resistance where heat enters at the right of the FG, which impedes thermal wavefront propagation [see inset in Fig. 5(b)] when compared to the previous case with no FG. Fig. 5(c) demonstrates the simulated heat transport in STI structures. The STI offers a high thermal resistance; thus, one can also notice heat diffusion in the transverse direction into the Si substrate. The effect is also manifested in the measured temperature rise.

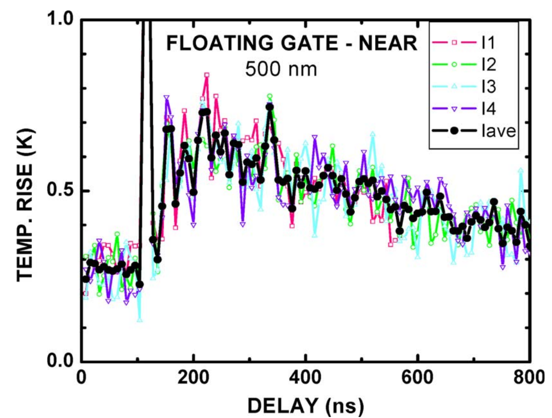

Fig. 6. Transient temperature rise sensed at the near junction in PC500. Four sweeps of overnight measurements and the average are also shown.

The developed pulse–probe technique was used to determine the temperature rise at the source junction, both in close proximity and rather farther from the heat source ("power" FET). Fig. 6 shows the results of the measurements of the temperature rise at the NEAR junction of the "sense" FET. The figure shows four consecutive measurements with a total duration of 10 h. Some of the fine structures are repeatable, indicating residual reflections. As expected, a smaller temperature rise and delayed response was detected when the current measurements were performed at the FAR junction [Fig. 7(a)] than in the previous case (Fig. 6). Although not shown, it is interesting to note that in the high-V_g mode, the NEAR-to-FAR signal ratio is $\sim$1. This is due to the fact that the high-V_g temperature sensitivity is based on the mobility changes, which makes it susceptible to the temperature throughout the channel of the FET rather than only at the source. The spatial resolution capability of the technique was used to investigate the impact of the FG on thermal transport. First, the temperature rise was measured at the NEAR junction in a set of device samples with FG of nominal gate length $L_g = 1100$ nm between the "power" and "sense" FETs. Thus, heat traverse through an external FG region of 1100 nm before detection. Second, the temperature rise was measured at the FAR junction in the test structures with FG of $L_g = 500$ nm. In this case, heat traverses through 500 nm of the external gate region of the FG and through additional 600 nm of the internal gate region of the "sense" FET as it reaches the FAR junction. The comparison of the temperature rise measured in these two cases is shown in Fig. 7(a). It is interesting to note that the gate regions of 500 nm (FG) and 600 nm ("sense" FET gate) have almost exactly the same combined effect on heat transport as the single gate region (FG) of 1100 nm. Fig. 7(b) shows the trend for the peak temperature rise $T_{\max}$ versus the total effective gate-region length available for heat transport. It also allows one to compare the NEAR and FAR junction measurements of the internal and external gate regions. It is clear from this plot that the peak temperature decreases with the increasing effective gate-region length. The latter was attributed to the higher values

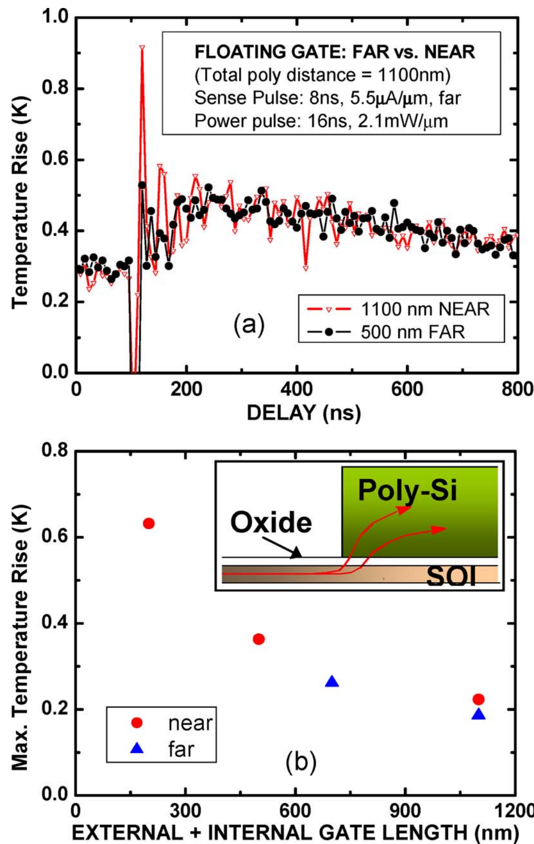

Fig. 7. Comparison of the temperature rise measured in PC500 at the far junction versus the temperature rise measured in PC1100 at the near junction. (b) Reduction in $T_{\max}$ rise measured as a function of the total gate region length. Inset shows the illustration of the heat diffusion into the gate.

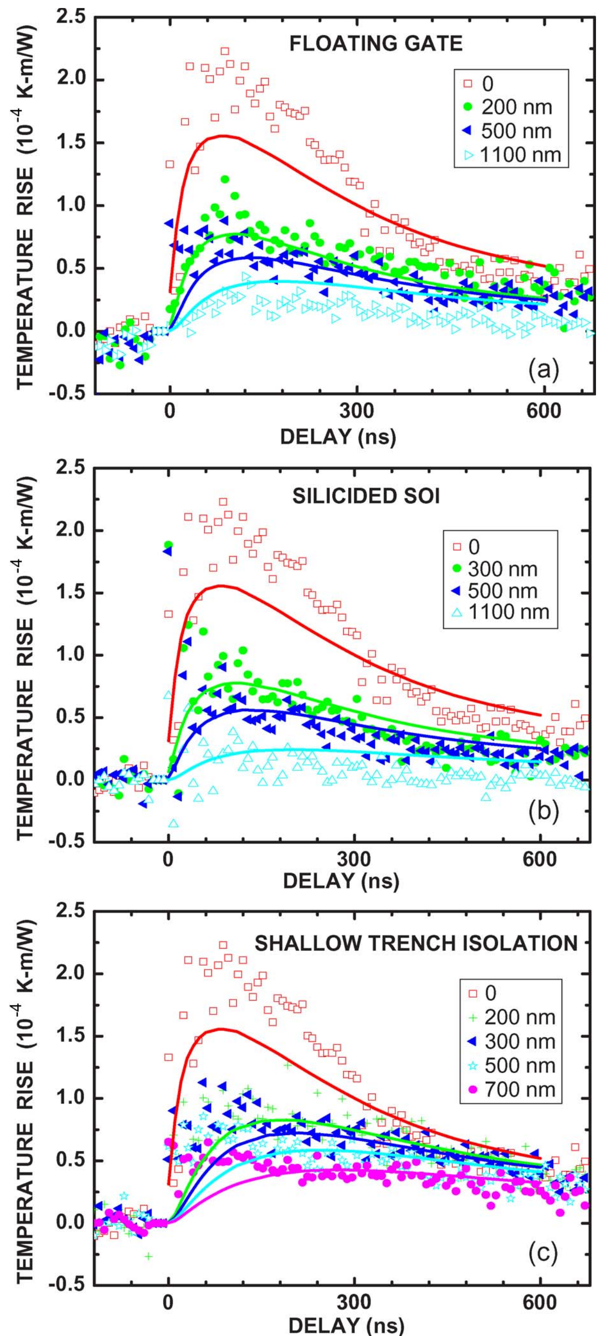

Fig. 8. Measured (symbols) and simulated (lines) transient temperature rise in no FG (OP0) and for different (a) FG lengths, (b) silicided SOI, and (c) STI structures.

of the thermal conductivity in the gate region, which results in faster and more efficient heat spreading.

The results of the measurements of the temperature rise at the "sense" FET reveal some interesting trends. The measurements of the temperature rise confirm that the sample with an SOI layer between the two FETs has the smallest rise time and decay time constants, followed by the FG and STI samples, which have STI between the two FETs. The temperature rise in the FG samples is lower than that in the OP structures. This is consistent with the data presented in Fig. 7, which indicate that the increasing effective gate-region length reduces the maximum temperature rise detected at the "sense" FET.

The simulated temperature rise at the FAR junction for FG structures is compared with the experiment in Fig. 8(a). The simulation shows heating and subsequent cooling in the structures with FG of gate lengths 200, 500, and 1100 nm. For comparison, the calculated and measured results for OP0 are also shown for the device without any intermediate structure between the "sense" and "power" FETs. The simulation results are in excellent agreement with the measurements for all the three considered FG samples. However, when the temperature decreases, the experimental decay time constant is smaller than its simulated value in the case of the FG samples with a large FG length (1100 nm). This could be due to the larger length of the gate region (as previously discussed, see Fig. 7), which improves heat spreading and conducts heat away from the SOI due to the higher κ of poly-Si. The temperature rise in the silicided structures with different separation distances between the "power" and "sense" FETs [Fig. 8(b)] was also measured and simulated. For the sample with the shortest separation distance (OP0, nonsilicide SOI), the simulations underestimate the peak temperature rise. This could be due to the differences in the actual and assumed values of 40 W/mK for the thermal conductivity of the silicide and SOI (40-nm layer thickness) [13]. The finite size of the simulation domain and selection of the boundary conditions also influence the numerical solution of the heat diffusion equation for transistor device structures [14]. Note that κ for a 10-nm SOI layer is expected to be ~90% less than that of bulk Si [13]. This reduction in κ has

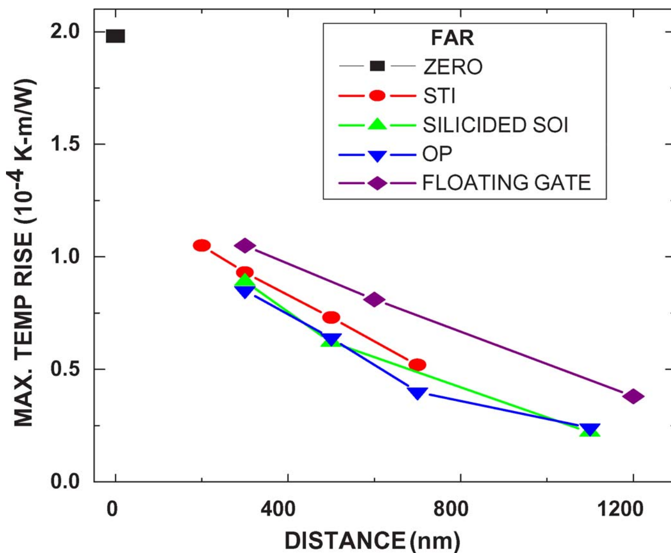

Fig. 9. Maximum temperature rise as a function of length of the medium between the FETs for the various media, as indicated.

experimentally been observed in thin SOI films with the thickness smaller than the phonon mean free path (MFP) in Si [15]. A typical value of the phonon MFP in Si at room temperature is 43–300 nm, according to different estimates and measurements [16]. The significant reduction of the thermal conductivity observed in SOI structures is mostly due to the phonon rough boundary scattering. Another factor contributing to the increase of the thermal resistance of the SOI structure along the vertical (growth) direction is the thermal boundary resistance (TBR) or Kapitza resistance [17]. Additional reduction of the thermal conductivity may appear in SOI structures with the thickness d much smaller than the phonon MFP as a result of the phonon confinement reduction of the group velocity [18]. In I structures, which have STI of different separation lengths between the two FETs, the measured temperature rise was surprisingly large, which is comparable to the OP and silicided structures. Examining the simulations in Fig. 5(c), one sees that heat actually shunts the oxide separating the devices by traveling through the substrate and transferring back into the device through the relatively thin buried oxide. However, the measured rise time is comparatively short. For example, in the device structures with a 200-nm STI separation length, the calculated rise time is ∼200 ns, whereas the measured rise time is ∼128 ns [Fig. 7(c)]. This suggest that the effective thermal resistance of the STI structure is smaller than the theoretical value. A larger set of the device test structures and more detailed heat diffusion simulations are needed to clarify this issue.

Fig. 9 reveals the differences in the thermal crosstalk through the different sets of materials and characterizes the ability of the structures to transfer heat. It shows the maximum temperature rise measured for the different lengths of the various media inserted between the FETs. The silicided structures appear to be thermally equivalent to the nonsilicided structures (OP) with respect to the heat transfer. One can also notice significant leakage of heat in the structures with STI separation of various lengths. The measurements show that the FG has the longest thermal attenuation length. At the same time, the temperature rapidly decays between the OP0 and the shortest FG point. This means that there is a thermal bottleneck to be overcome for the transmission of heat into the FG from the SOI layer. This can also be understood from the previous discussion of Fig. 5(b), which notes that the additional thermal impedance may be due to the TBR at the interface of the 1.2-nm gate oxide layer [17], [19], [20].

VI. Conclusion

A new experimental technique has been developed to investigate the transient thermal crosstalk between FETs implemented on SOI substrates. Owing to its superior temperature and time resolution, the technique can measure the temperature rise at different junctions of the devices, thus achieving a very high spatial resolution in temperature mapping. The finite-element simulations of heat diffusion in the devices were performed to calculate the temperature rise and compare them with the measured values. The simulations clearly show significant lateral spreading of heat wave to the neighboring devices, which gives rise to the measurable thermal crosstalk. The measurements and simulations confirm the thermal crosstalk through all the materials and structures tested, including the STI, making it difficult to achieve adequate thermal isolation in very sensitive analog-type or sense amplifier applications when the heat source is close. On the other hand, efficient heat transfer to the gate allows even thin SOI devices to be efficiently cooled. Such measurements, as the one described here, help determine the interface transfer resistance, which is important for determining the internal FET temperatures. The experimental and simulation technique can be extended to studying thermal transport within a submicrometer CMOS FET and is capable of detecting and resolving the hot spots inside a single transistor. The high-resolution experimental–simulation approach is important for the design of high-density devices, where thermal crosstalk is expected to be a major design challenge.

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